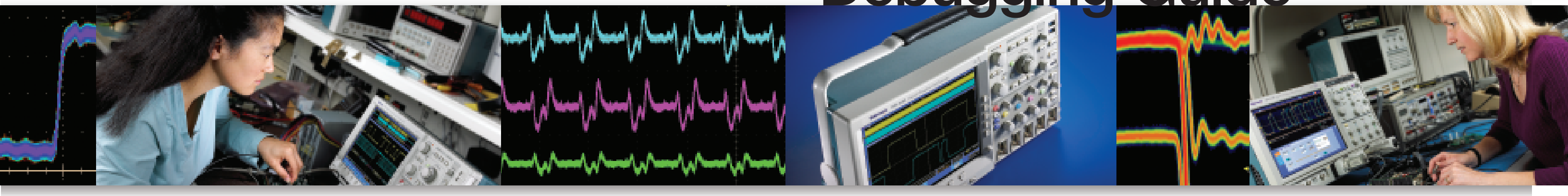
Digital Design

Debugging Guide



Tektronix

Enabling Innovation

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Introduction

As system speeds increase and designs shrink, it is harder for circuit designers to preserve a signal's ideal digital characteristics. The higher speed and denser designs in their designs introduce an array of unintended electrical events that impact a circuit's operation. Part placement, trace-run placement, noise and small signal variations take on a larger role in high-speed designs. For example, when circuits perform at frequencies in the gigahertz range, the inductance of a trace plays a larger role in the design.

Engineers must quickly find and analyze noise, set up and hold violations, glitches, metastability issues, bus contention, jitter and other signal problems. Many digital problems are easier to pinpoint when observing a signal's behavior and seeing an analog representation of a problematic high-speed digital signal.

While the problem may appear as a misplaced digital pulse, the cause of the problem signal could be related to the signal's analog characteristics. Analog characteristics can become digital faults when low-amplitude signals turn into false logic states, or when slow rise times cause pulses to shift in time. Seeing a digital pulse stream with a simultaneous analog view of the same pulses is the first step in debugging these problems.

Digital oscilloscopes, like the DPO4000 and DPO7000 series, are debugging tools that can help engineers troubleshoot their high-speed embedded system designs. Keep in mind that when viewing signals small details can make a big difference to the signal appearance and the accuracy of a measurement.

Tracking Down Noise

Noise is any unwanted signal in a digital system. Transmission lines, ground bounce, reflections, crosstalk, ringing, wave propagation are all noise problems that denser and speedier chips bring to today's circuit designs. With logic having faster rise-times (slew rates of several volts/ns), engineers are commonly debugging high-speed designs with rise times over 1 ns.

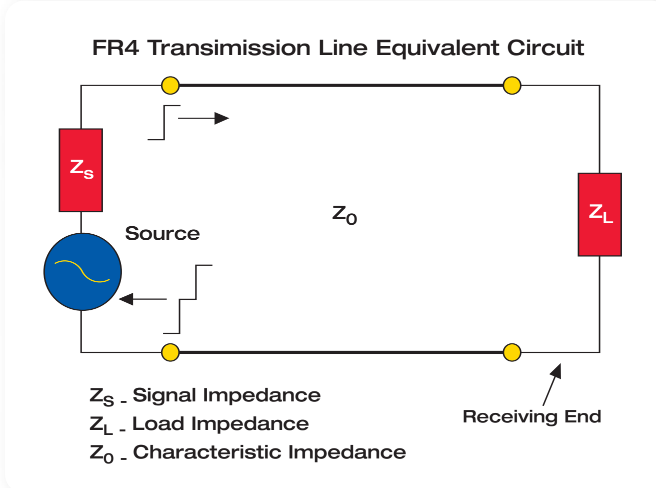
Transmission Line Effects

Treat a connection like a transmission line when the propagation of the signal down the line and back is longer than it takes to complete the transition (when $2T_{prop} > T_{rise}$).

For a typical circuit board of FR4 material, the propagation speed is roughly 15 cm/ns. With a 1 ns rise time, any trace longer than 7 cm can have transmission line effects. The source and destination (receiving end) signals are often different because of reflections and ringing. When measuring signals of these speeds, it is important to probe the receiving end of the line (Diagram 1).

Ringing and Reflections

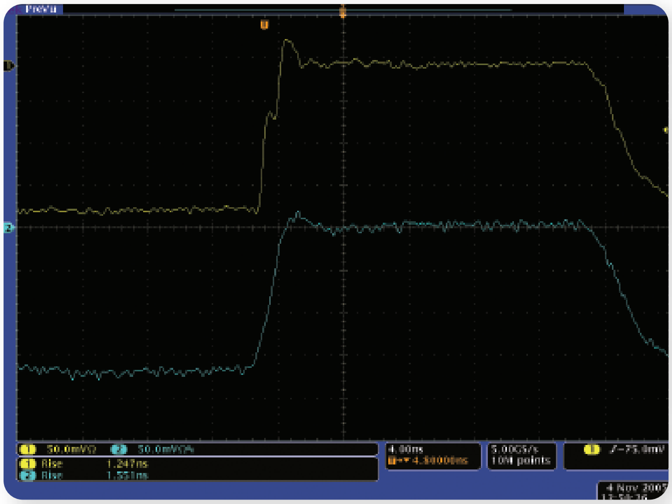
An under damped resonant circuit can cause ringing and overshoot. Inadequate power supply bypassing, attaching long power and ground leads to the device, and poor probing techniques can all introduce ringing and overshoot. Reflections from mismatched or unterminated lines can result in glitches or other disruptions in the transition.



▶ **Diagram 1.** *A transmission line equivalent circuit shows how an impedance mismatch produces a signal reflection.*

These effects can cause unwanted state-transitions or timing uncertainty. Some digital circuits repeat patterns infrequently. A digital oscilloscope with adequate bandwidth and sampling rate easily captures these non-repetitive events in real-time.

Probes and probing techniques affect the quality of a measurement. High capacitive loading can slow down signal edges, masking some problems while creating others. Touching a probe to a circuit node can cause a symptom to disappear. Inductance from the probe ground-lead and capacitance from the probe input form a series-resonant circuit that appears as ringing unless the resonant frequency is pushed above the oscilloscope bandwidth.



▶ **Figure 1.** *The top signal (Ch 1) shows a 1.3 ns rising edge captured with a 1 GHz DPO4000. The bottom signal (Ch 2), is identical to the top but its bandwidth limited to 250 MHz showing what a 250 MHz oscilloscope might display. The reflection in the signal is masked by the insufficient bandwidth. (Note how insufficient bandwidth produces inaccuracies in signal rise time.)*

Shortening the probe's ground lead and lowering the input capacitance raises the resonant frequency. Loading capacitance for conventional probes may be as high as 10-15 pF. An active probe reduces this problem. For example, the 2.5 GHz TekVPI™ Active Probe has a <0.8 pF of input loading capacitance. This capacitive difference keeps the ringing down and allows using longer ground leads.

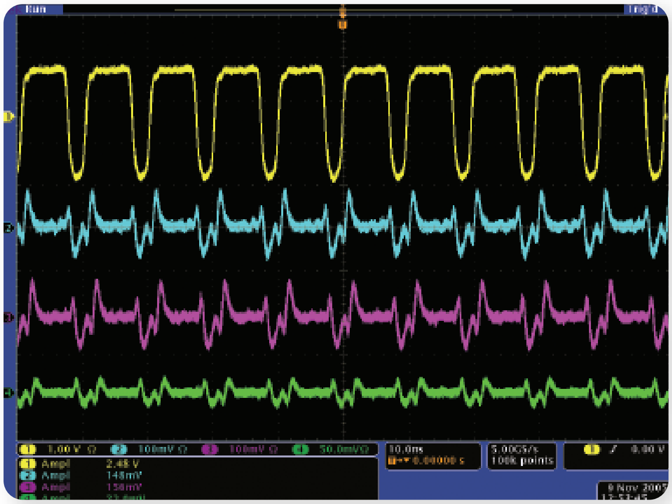
Figure 1 shows the importance of bandwidth and sample rate for viewing a reflection. The rising transition has a reflection within the transition region. For a clock signal, this could cause timing uncertainties, or jitter, in the clocked output. The top trace (Ch 1) was acquired with a 5 GS/s DPO4000 with 1 GHz bandwidth. To display the results on a lower performance oscilloscope, the bottom trace (Ch 2) was acquired at 5 GS/s with a 250 MHz filter. To see the disruption of the transition, the DPO needs the appropriate sample rate and bandwidth.

▶ **Figure 2.** *Ground bounce from switching output on channel 1.*

Ground Bounce

Ground bounce is a shift in a device's ground reference caused by a current spike in its ground plane. When multiple outputs on a device switch synchronously, they can generate large transient ground currents. The voltage drop across the bond-wire, ground-lead and the return path cause the ground potential inside the device to "bounce" above system ground. Excessive ringing or glitches in switched or unswitched outputs may cause unwanted transitions in other devices. A ground bounce may even cause the device to drop data.

In Figure 2, Ch 1 captures one output of a 74LVC00 Quad AND gate. Three AND gates in the quad package each have one input tied to the +3.3 supply voltage and the fourth AND gate has its input tied to ground. The four remaining AND gate inputs receive a 48 MHz signal. Ch 2 observes the device that is not switching. Because of ground bounce, Ch 2 shows slightly over a one volt peak-to-peak disturbance. Analyzing the signal on Ch 2 shows why the bounce on Ch 2 is larger on the falling edge of the corresponding Ch 1 than on the corresponding rising edge of Ch1.



▶ **Figure 3.** *An example of crosstalk captured using edge trigger on the DPO4000 1 GHz bandwidth oscilloscope. The fast pulse on one of several parallel 50 ohm traces (Ch 1) generates high energy radiations. These aggressors can be induced into nearby traces. This is clearly evident on Ch 2 and 3, the traces nearest to the aggressor. As the distance from the aggressor trace increases the crosstalk diminishes. This is shown on Ch 4 by the 32 mV amplitude, the farthest parallel victim trace from the aggressor.*

Electrically, looking into the output of the AND gate with one input tied to ground provides almost a direct path ground except for a small amount of equivalent inductance. The switching outputs of the three AND gates cause current flow which induces current into the output of the non-switching AND gate into the equivalent inductance causing the larger spike on Ch 2. Note that if the AND gate with the input tied to ground was tied to supply voltage, the larger spike would occur on the rising edge of Ch 1.

Crosstalk

This is often an issue in digital designs where asynchronous lines couple into clock lines. Crosstalk causes false transitions or "pulls" clock edges producing timing errors or setup and hold violations. The program worsens as rise times get faster. Long probe ground-leads can fool you into seeing "false" crosstalk, because long leads can create large circuit-loops.

When observing crosstalk on an oscilloscope consider: number of channels, sample rate, and bandwidth. To capture a signal in real-time on your DPO set an adequate sample rate on all channels.

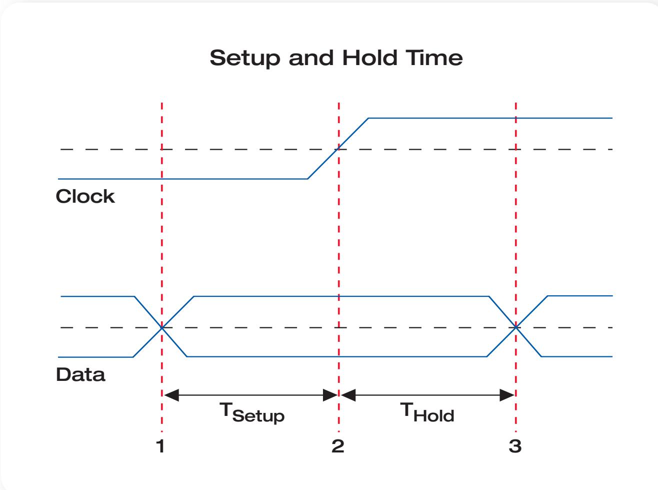
For example, when a fast-transition signal on a circuit-board run couples (capacitively and inductively) to a nearby signal path, it creates crosstalk.

There are three modes of crosstalk to consider during debugging: Inductively (or transformer) coupled crosstalk, reverse crosstalk and forward crosstalk.

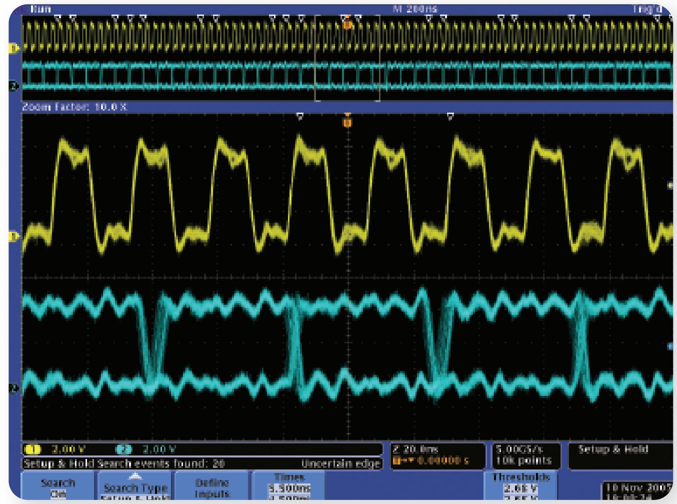
Inductively or transformer coupled crosstalk occurs when a pulse propagates on a line (aggressor) changes the next location with a current spike that induces a magnetic field. This magnet pulse in turn induces a current spike on a second line (victim). The transformer creates two opposite-polarity voltage spikes in the forward direction and positive spikes in the reverse direction.

Reverse crosstalk is the sum of the same polarities in the victim line spreading in the source direction. It is seen as a low-level, wide pulse with the width relative to the line length. Reverse crosstalk amplitude is independent of the aggressor-pulse rise-time. It depends on the mutual-impedance value.

Forward crosstalk is the sum of two opposite polarity pulses that depend on the relative values of the capacitance and inductance. It propagates towards the original aggressor line. It can be seen at the end of the victim line as a narrow spike and width of the aggressor-line rise time. The faster the aggressor-pulse rise time, the faster the rising edge, the higher the amplitude and the narrower the pulse shape. Forward crosstalk depends on the paired line length. As the crosstalk location propagates along the aggressor pulse-edge, the forward crosstalk in the victim line receives more energy.



▶ **Diagram 2.** *This diagram describes Setup time (T_{setup}) and Hold time (T_{hold}) definitions for a clocked logic circuit. Setup time is measured between points 1 and 2. Hold time is measured between points 2 and 3.*



▶ **Figure 4.** *The DPO4000 combines Search and Mark features with specialized Setup and Hold triggering. At the top of this display, the white hollow triangles mark all setup and hold violations with the user defined setup and hold times of 5.5ns and 4.5ns respectfully.*

Preventive Measures

The DPO4000 with 2 GS/s sample rate on all four channels, 500 MHz bandwidth and an active probe is ideal for uncovering the analog effects .

Keep in mind these things for digital designs:

- Keep signal runs short.
- Consider transmission line effects when the propagation delay of the run is more than half the rise time.
- Power and ground planes, coupled with effective bypass capacitors, can eliminate many problems with ringing and crosstalk.
- When there are problems, make sure that the oscilloscope has enough bandwidth and sample rate on all four channels to observe the event effectively.

Finding Setup and Hold Violations

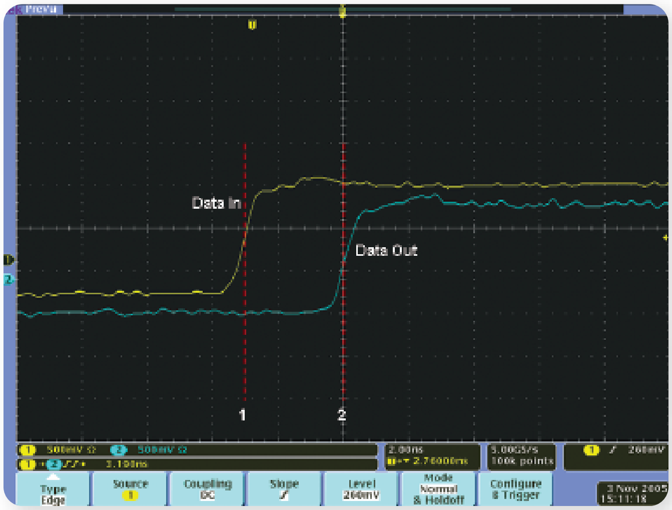
Digital systems contain clocked logic devices from flip-flops to microprocessors. Each has its own setup and hold time specified by its manufacturer.

Increase a digital system's speed and the data stabilization time before to the clock signal decreases. Setup is the time an input signal must be stable (valid) before the clock edge. Hold is the amount of time that data must be stable after the clock edge so that data is valid data at the output. See Diagram 1, setup and hold time.

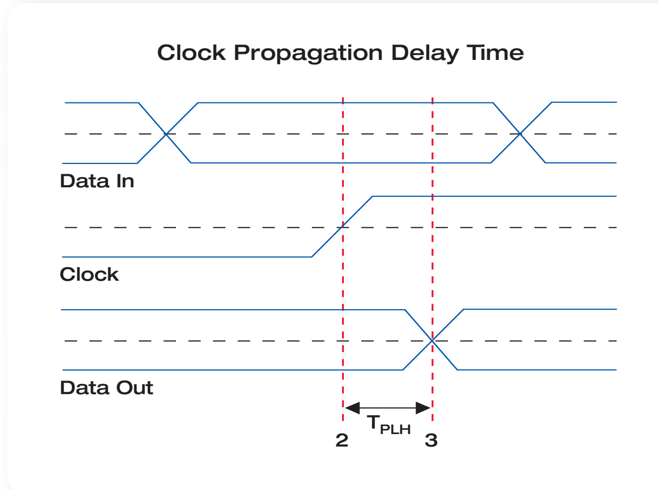
In Figure 4, the setup time is between point 1 of the data and point 2 of the clock. The minimum setup time specified by the manufacturer is 5 ns. The hold time is measured between point B of the clock and point C of the data. The minimum hold time specification is 4 ns.

Whenever a signal changes between a device's setup and hold, it creates a system fault, or a setup/hold violation. Crosstalk and reflections on clock and data signals degrade signal integrity and produce these violations. As devices run faster their setup and hold times decrease. This makes their timing relationships harder to debug.

Violations of setup or hold requirements can cause unpredictable glitches on the device's output, or no output transition at all. The SETUP/HOLD trigger on a digital oscilloscope allows triggering on both setup and hold times between the clock and data signals present on any two oscilloscope input channels. With the digital signals viewed on the DPO, the precise timing measurements of setup and hold violations can be seen.



▶ **Figure 5.** *The DPO4000 uses its delay time measurement capability to measure and display a propagation delay time, from Data In rising edge (point 1) to Data Out rising edge (point 2), to be 3.190ns.*



▶ **Diagram 3.** *These signals illustrate the propagation time high-to-low (T_{PLH}) and for a clocked logic circuit is measured between points 2 and 3.*

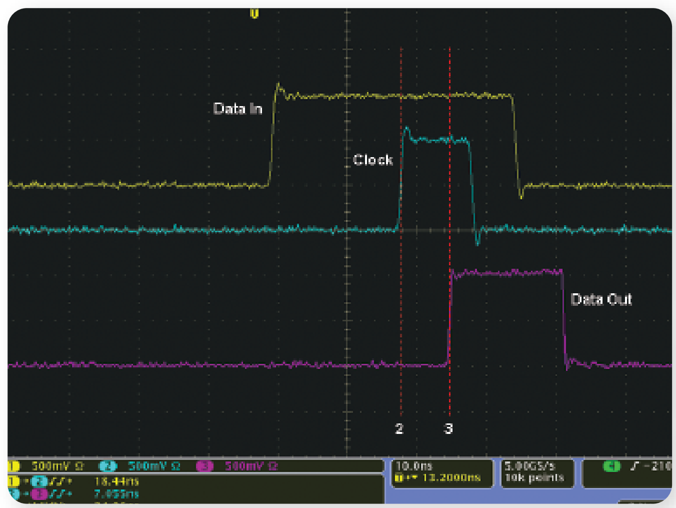
Propagation Delay

It takes time for signals to travel from one point to another in a system—from the input of a circuit to its output, or from the output of one device to the input of the next device. This time is the propagation delay of the signal path. It is common for a circuit to have two different propagation delay specifications depending on the polarity of the signal change. These specifications are represented as t_{plh} (propagation low to high), t_{phl} (propagation high to low).

Gated Propagation Delay

For a logic gate, the propagation delay is the time a signal needs to pass from the input to the output of the gate. The propagation delay specification for the device captured in Figure 5 is measured between Data In signal (point 1) and Data Out signal (point 2).

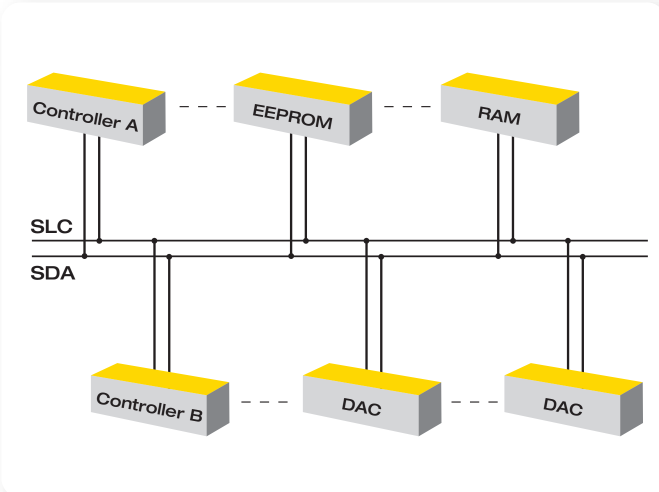
The DPO4000 oscilloscope captures the input and output data waveforms of an AND gate IC in Figure 5. Where the Ch 1 probe is on Data In and Ch 2 probe is on Data Out. Using the delay time measurement capability, the measurement time variables are selected from the first rising edge on Ch 1 to the first rising edge on Ch 2. The DPO measures and displays the propagation delay time of 3.190 ns.



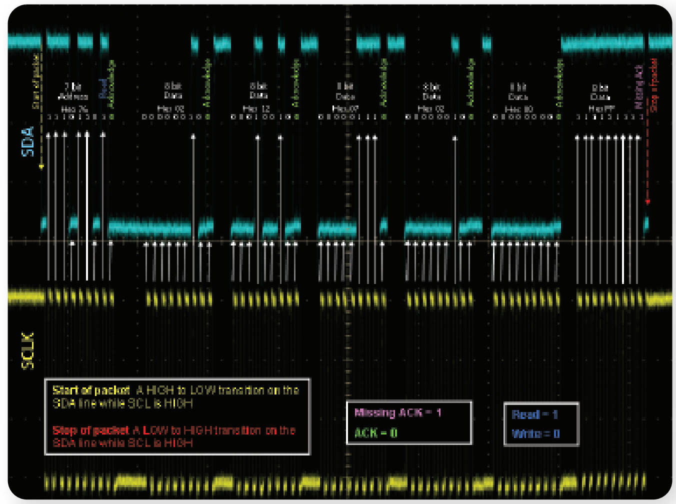
▶ **Figure 6.** *The flexibility of the DPO4000 delay time measurement setup capability is used to measure clocked propagation delay time—this is the time measured between Data Out rising edge (point 3) with respect to the Clock rising (point 2). The clock propagation delay time is 7.055 ns.*

Clocked Propagation Delay

For a clocked circuit, like a flip-flop or a latch, the clocked propagation delay is the time needed for the active clock-edge to change state at the output of the circuit, or its CLK to Q propagation delay. The flip-flop in Diagram 3 has a maximum low-to-high propagation delay (T_{PLH}) of 8 ns. In other words, no more than 8 ns after the clock goes high, the output will change to the state of the input data.



▶ **Diagram 4.** *Diagram of I²C bus with various connected devices each selected by a unique address identifier contained in each serial packet transmitted.*



▶ **Figure 7.** *A DPO display shows I²C Bus hand decoding. The address is 76, the operation is a read.*

The oscilloscope display in Figure 6 shows the data captured by a DPO4000. The DPO was set to sample at 5 GS/s with Ch 1 attached to Data In, Ch 2 attached to Data Out. The digital oscilloscope triggers on the rising edge of Data In and Ch 2 attached to the clock input.

Solving Bus Contention Problems

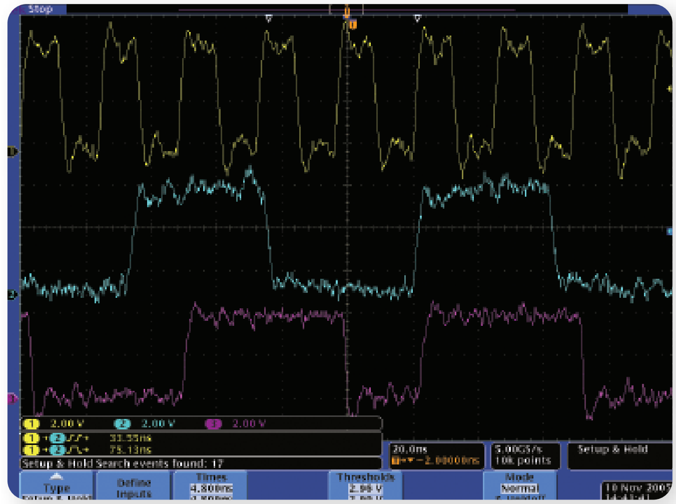
Circuit devices such as DSPs, RAM, EPROMs, PROMs, ROMs A/D and D/A converters and I/O devices commonly communicate to the outside world over low and high-speed serial-buses. Bus contention is one example of how these buses are more difficult to debug than parallel buses. The low-speed serial-bus in Diagram 4 is the I²C bus standard layer and protocol developed by Philips Semiconductor.

Most digital oscilloscopes, like the DPO4000 or DPO7000 Series, will trigger on logic signal combinations described as either pattern or state signals. Figure 7 illustrates how engineers have had to decode I²C serial buses, bit by bit; first finding the Start of Packet transition; then the first seven bits of the first byte is the address; then looking at the eighth bit of the first byte determines if it is a read or write, and decoding the data up to eight bytes. Some serial buses, like CAN bus, are impossible to decode by hand because of bit correction.

▶ **Figure 8.** *The DPO4000 I²C Bus triggers on selected address 76 for a read or a write. Each packet is easily decoded eliminating hand decoding, reducing errors and saving time.*

The optional I²C, SPI and CAN bus triggers on the DPO4000 permit debugging bus contention by triggering on signals specific to these buses at rates up to 10Mbits/s. Using these triggers you can set up expected bus patterns. For example, on an I²C bus you might want to trigger on the start or end of a packet, the type of frame (data, remote, error or overload), a standard or extended identifier, or even a missing acknowledgment. DPO4000 can trigger and search on most common packet information.

▶ **Figure 9.** *A DPO display shows time qualified pattern triggering for a device. The input line for Ch 3 should be high when the signals on Ch 1 and Ch 2 go high. Setting Ch 3 to a low state uncovers an added delay problem.*



▶ **Figure 10.** *Using the DPO4000 Setup and Hold Trigger and the Search/Mark capability show metastable states noted by the white triangles at the top of this display. Ch 1 is the clock signal and Ch 2 the data signal. Channel 3 is the metastable Q output of a D-type flip-flop latch.*

Pattern Triggering

A pattern is only valid when a combination of logic levels is at the required level and remains there throughout an event. The user determines whether to trigger the DPO when the pattern goes true (as it enters the condition set) or when it goes false (as it exits the condition set).

State Triggering

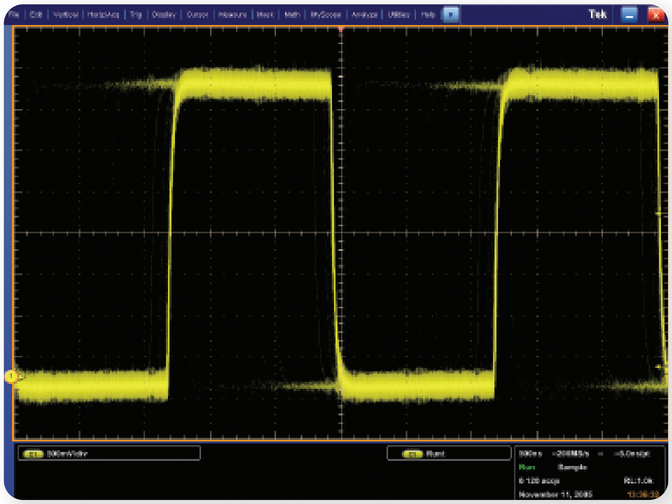
In synchronous systems (i.e. qualified by a system clock), state triggering can qualify the triggers. Using a similar bus example, change the receiving buffer to a latching buffer. Figure 9 shows how a time-qualified pattern-trigger allows each of the device inputs to set a state. Ch 3 is set to a low state. Ch 1 and Ch 2 are set to high.

The problem state is captured, discovering the problem of too much delay for the signal on Ch 3. The input line for Ch 3 must be high when the input lines on Ch 1 and Ch 2 go high, for the clock to latch the correct. Obviously, this only works in a system where the control signals of the various devices and addressing the bus are synchronized to a master clock.

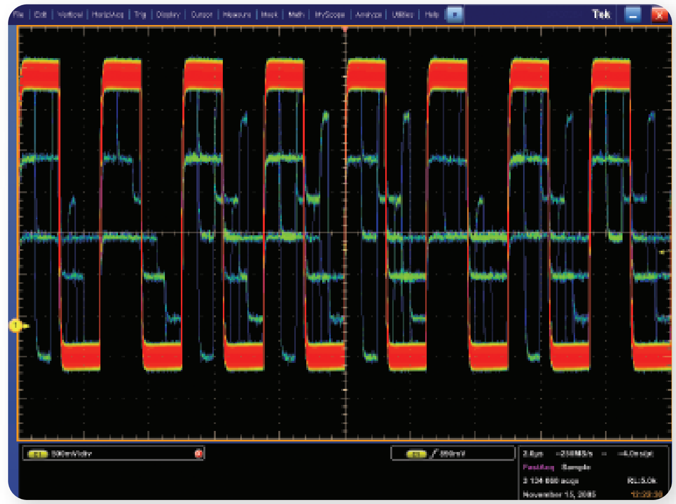
Capturing Metastable Events

Metastability is an indeterminate or unstable data state. The resulting output signal may be a glitch that causes problems. Such states usually occur infrequently making them more difficult to detect and capture than other phenomena. Metastable states can be caused by setup and hold violations at the input of a latching circuit, such as the D flip-flop in Figure 10.

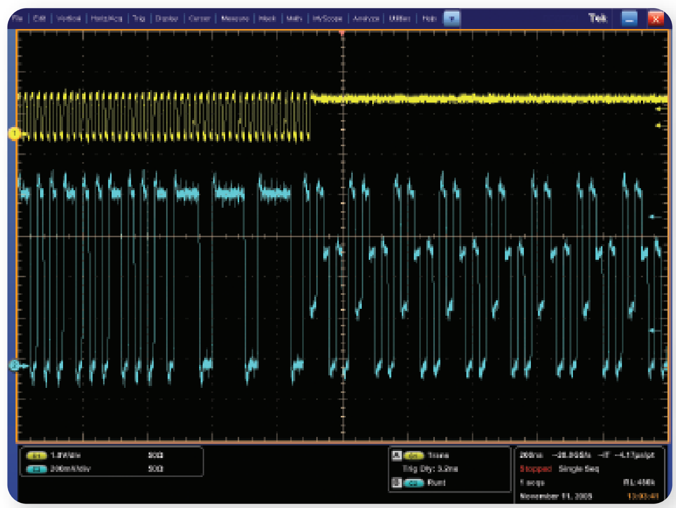
Figure 11 shows the DATA and CLOCK signals to the flip-flop run asynchronously. Sometimes the rising edge of the clock occurs as the data changes state causing a setup and hold violation. This may vary the output of the flip-flop, which might stay at its original state, reflect the change in the data or hesitate between these states. During this momentary “hesitation,” the flip-flop becomes metastable and the output of the flip-flop (Q or /Q) becomes chaotic.



▶ **Figure 11.** *A digital oscilloscope can show signals like they really are letting designers see how glitches affect design. Above the DPO7000 display shows very intermittent signal glitches using persistence. A persistence display generates a visual trace history.*



▶ **Figure 12.** *It is easy to see potential runt and transition-error conditions with the DPO7000 FastAcq acquisition mode.*



▶ **Figure 13.** *The DPO7000 Pinpoint™ trigger makes it possible to use sophisticated trigger types for the B event as well as the A event. Here a B event is defined like A to isolate one bad transition followed by another. No matter if the B event arrives soon after an A event or much later. Either causes an acquisition. Runt logic pulses never cross through all the threshold levels necessary to become valid.*

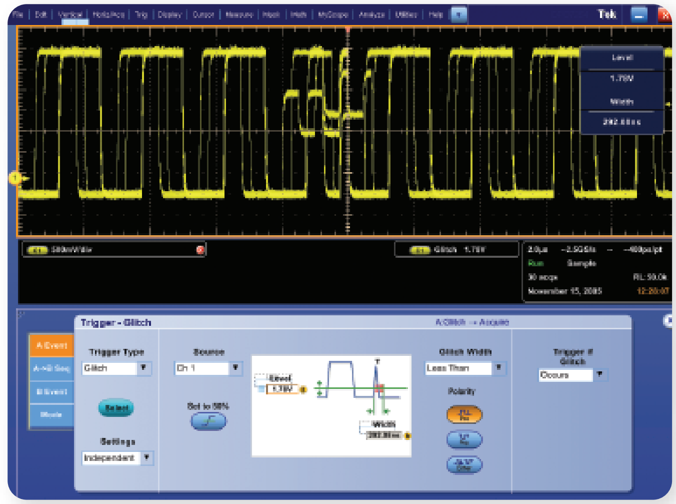
In Figure 13, the flip-flop fails to latch data causing it to fall back to its previous state. Undetectable with normal triggering, event triggering can reliably capture metastable states, a transition to runt in this case. Both transition and runt triggers use dual-amplitude threshold qualification to capture metastable signals.

Metastability, like other difficult debug problems, can also benefit from complex triggering. Pinpoint triggering in the DPO7000 provides one of the most comprehensive triggering mechanisms available for debugging designs, because it's useful to the full bandwidth of the oscilloscope. Pinpoint triggering performance and features uncovers elusive behaviors in prototypes.

Catching Glitches

A glitch is a generic term for any deviation from the idea digital waveform. Glitches are very narrow and fast unexpected pulses that a system might interpret as logic changes. Glitch problems are caused by many types of errors and can be difficult to debug. Their effect on system operation is unpredictable. Most design problems appear as glitches in one or more of the signals. Often they are the first sign of a variety of device faults, including noise, race conditions, termination errors, driver errors, crosstalk and setup/hold or other timing violations.

▶ **Figure 14.** *With the DPO7000 Glitch Trigger, an infrequent metastable state is captured at the Q output of a D-type flip-flop.*



▶ **Figure 15.** *Glitches may go undetected when a digital oscilloscope is not acquiring data. Higher update rates decrease the time necessary to capture glitches.*

Fast digital edges contain high frequencies that make proper termination of circuit board traces important in designs. They can cause larger transient currents that result in increased dynamic currents causing problems such as ground bounce or power distribution glitches. Fast edges can also increase crosstalk. Circuit board traces that in the past were treated as lumped circuit traces are now transmission lines that need proper termination.

If a circuit is malfunctioning, checking for glitches is a good place to start debugging. See what the glitch looks like by comparing the analog and digital representations on the digital oscilloscope. Most problems will appear as glitches in at least one, if not more, of the signals.

For example, the DPO might display a distortion on both the rising and falling edges of a digital pulse. The rising edge does not drop low enough to trigger a logic transition and so doesn't appear as a glitch. With a digital oscilloscope, like the DPO7000, and pulse-width triggering, capturing such intermittent glitches in order to trace the fault to its source is helpful.

Picking Out Jitter

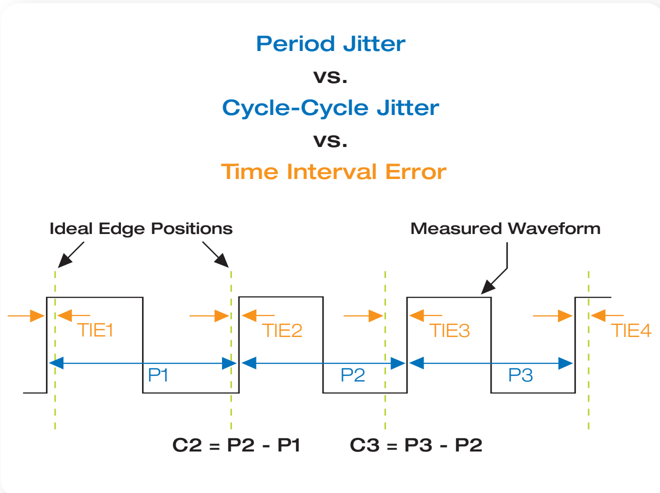
An unwanted timing variation in any series of clock or data pulses is called jitter. Jitter occurs in all electrical systems that use voltage transitions to represent timing information. It is the short-term variations from a digital signal's ideal positions in time. As a random process, jitter degrades systems performance and eludes debugging efforts.

Rapid timing variations occurring during the period or phase of either adjacent or non-adjacent pulse edges cause jitter. More simply, jitter is the deviation of timing edges from their "correct" locations.

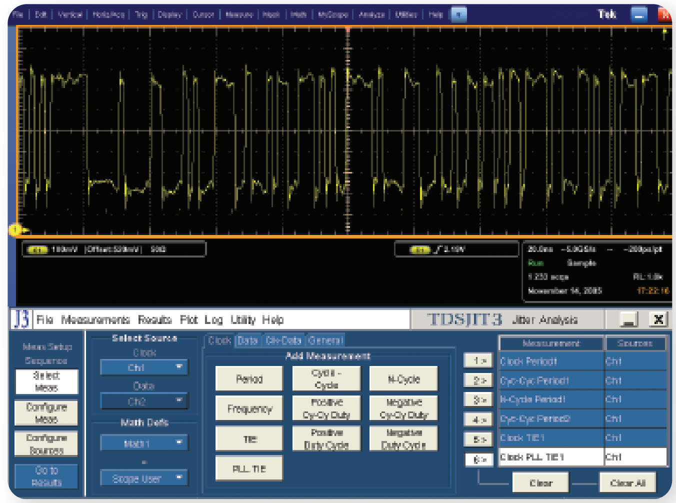
There are three common ways to measure jitter on a waveform: period jitter, cycle-cycle and time interval. Diagram 5 shows these measurements relate to each other.

Period jitter is simply the measurement of the period each clock cycle in a waveform. Triggering the oscilloscope in the first edge of the single will show the period jitter on the second edge.

Diagram 5 shows a clock-like signal with timing jitter. The dotted lines depict the ideal edge locations, corresponding to a jitter-free version of the clock.



▶ **Diagram 5.** *Above shows a clock-like signal showing timing jitter. The dotted lines are the ideal edge locations, corresponding to a jitter-free version of the clock.*



▶ **Figure 16.** *When a DPO7000 runs TDSJIT3 application on complex signals, sophisticated Jitter Analysis measurements are made rapidly for the design engineer to analyze.*

Cycle-cycle jitter measures how much the clock period changes between any two adjacent cycles.

The cycle-cycle jitter, indicated by C2 and C3 in Diagram 5, measures how much the clock period changes between any two adjacent cycles. As shown, the cycle-cycle jitter can be found by applying a first-order difference operation to the period jitter.

This measurement can be of interest because it shows the instantaneous dynamics a clock-recovery PLL might be subjected to. No information about the ideal edge locations of the reference clock was required to calculate either the period jitter or the cycle-cycle jitter.

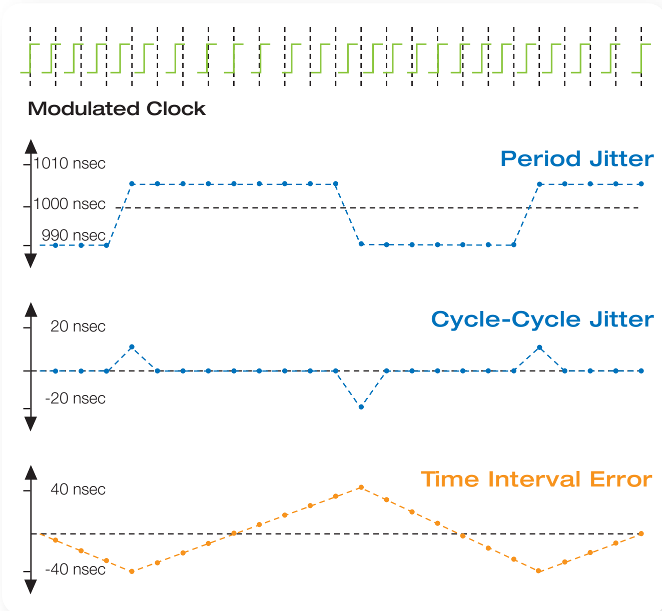
Time Interval Error (TIE) measures how far each active edge of the clock varies from its ideal position. To perform this measurement, you must either know or estimate the ideal edges. This is an important measurement because it shows the cumulative effect that even a small amount of period jitter can have over time.

The period jitter, indicated by the measurements P1, P2 and P3 in Diagram 5, simply measures the period of each clock cycle in the waveform. This is the easiest and most direct measurement to make.

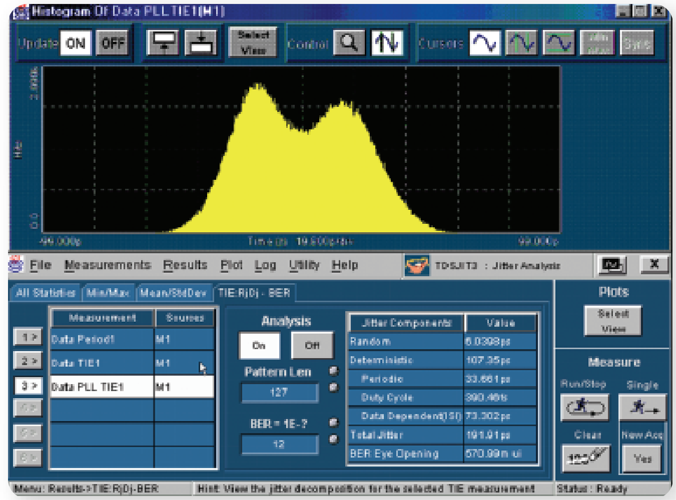
The peak-to-peak value may be estimated by adjusting the DPO to display a little more than one complete clock cycle with the display set for infinite persistence. If the scope triggers on the first edge, the period jitter can be seen on the second edge, as Diagram 5 shows.

The time interval error is shown in Diagram 5 by the measurements TIE1 through TIE4. The TIE measures how far each active edge of the clock varies from its ideal position. To perform this measurement requires that the ideal edges be known or estimated. It is difficult to observe TIE directly with an oscilloscope without some means of clock recovery or post-processing is available.

The TIE may also be obtained by integrating the period jitter, after first subtracting the nominal (ideal) clock period from each measured period. TIE is important because it shows the cumulative effect that even a small amount of period jitter can have over time. Once the TIE reaches ±0.5 unit intervals, the eye is closed and a receiver circuit will experience bit errors.



▶ **Diagram 6.** *How three jitter measurements—period, cycle-to-cycle and time interval—compare to each other on the same waveform.*



▶ **Figure 17.** *DPO7000 with the TDSJIT3 Jitter Analysis application reveals a total jitter on the data signal equal to ~192 ps (Tj = Dj + 2Q(BER) * Rj), where Q(10E-12) = 7. The associated histogram of data PLL TIE measurement provides an engineer with a graphic representation of the data signals statistical distribution.*

Diagram 6 gives an example of how these three jitter measurements compare on the same waveform. In this example, the waveform has a nominal period of 1 µs, but the actual period follows a pattern of eight 990 ns cycles followed by eight cycles of 1010 ns.

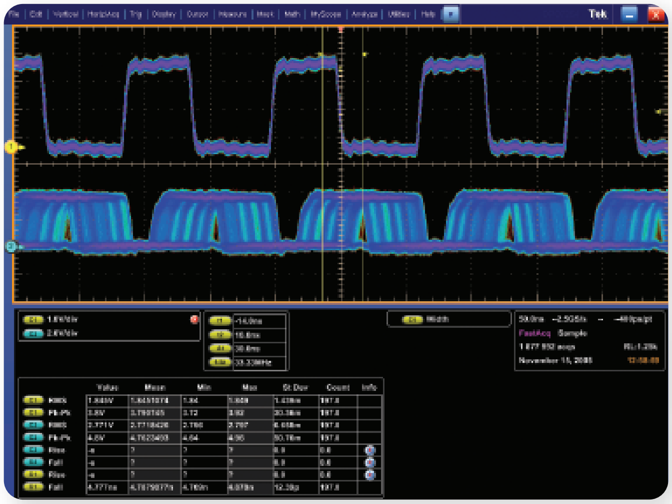
All jitter has both random and deterministic components. Because of the random components, jitter is best specified using common statistical techniques. Metrics such as mean value, standard deviation, and peak-to-peak value, with qualifiers such as confidence interval, are used to establish meaningful and repeatable measurement results.

Deterministic Jitter (Dj) is timing jitter that is repeatable and predictable. The peak-to-peak value of Dj is bounded, and the bounds can be observed or predicted with high confidence based on a relatively low number of observations. Dj is caused by:

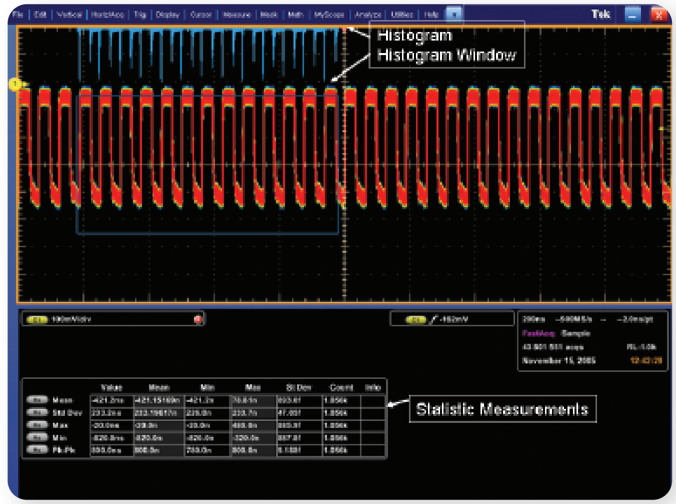
- Periodic jitter (Pj) is due to repetitive noise sources like power supplies, adjacent oscillators and in some cases crosstalk of adjacent buses.
- Duty Cycle Distortion (DCD) is caused by an imbalance in the drive circuit bias levels or thermal effects within the transmitting device.
- Inter Symbol Interference (ISI), also called Data Dependent jitter (DDj), is caused by frequency related losses in the signal path, most commonly because of interconnect and cabling losses.

Random jitter (Rj) is timing noise that has no discernable pattern and is not readily predictable. The primary source of random noise in electrical circuits is thermal noise (Johnson noise or shot noise). RJ is assumed to have a Gaussian distribution and there is no bounded peak-to-peak value for the underlying distribution—the more samples taken, the larger the measured peak-to-peak value will be.

Periodic jitter (Pj) repeats in a cyclic fashion. Since a periodic waveform can be decomposed into a Fourier series of harmonically related sinusoids, this kind of jitter is sometimes called sinusoidal jitter. Pj is typically caused by external deterministic noise sources such as switching power-supply noise or a strong local RF carrier. It may also be caused by an unstable clock-recovery PLL.



▶ **Figure 18.** *DPO7000 handles up to eight automated measurements at one time, including Rise, Fall, and Pk-Pk. Simply setting the cursors on the measurement points of interest produces the results.*



▶ **Figure 19.** *The FastAcq acquisition mode on the DPO7000 with statistical measurements selected and displayed shows relatively stable clock signal on Ch 1. The histogram region is selected and turned on demonstrates how easily and rapidly design engineers can employ statistical analysis tools for confidence in compliancy.*

Data-dependent jitter (DDj) is any jitter that is correlated with data-stream bit sequences. DDj is often caused by the frequency response of a cable or device. Another common name for DDj is pattern dependent jitter (PDj). It is the measured result of inter-symbol interference (ISI).

Duty Cycle Distortion (DCD) is the variation in duty cycle from the nominal value of 50 percent. There are two common causes of DCD: the slew rate for the rising edges differs from that of the falling edges; or the decision threshold for a waveform is higher or lower than it should be because the signal DC average has shifted.

Total jitter at Bit Error Ration (Tj @ BER) is the estimate of the peak-to-peak jitter at the user defined bit error ratio. When combined with the unit interval, the predicted eye opening estimated at BER is also estimated and displayed in the BER bathtub curve plot.

Automated Measurements and Analysis

For higher speed signals automated measurements and statistical analysis can provide insights into debugging the design. Many automated measurements and statistical analysis in today's digital oscilloscopes provide the flexibility and level of performance needed for debugging tasks. Displaying either four or eight waveforms at a time, allows comparing and scrolling through waveforms to see their relationship.

Automated, push button, measurements allow engineers to observe problems in new ways by gathering measurement statistics, defining reference levels, and then bringing the oscilloscope's flexibility and performance to bear on the debugging task. By capturing and comparing multiple measurements on-screen, the DPO displays the statistics of each and where differences might be.

This way an engineer can see whether components are operating within their specified ranges or if their tolerances vary and need correcting.

Common automated measurement helpful for speeding up debugging include pulse width, overshoot, duty cycle, overshoot, peak-to-peak, as well as more complex statistical measurements such as minimum, maximum and root mean square (RMS).

Automatic Jitter and Timing Analysis

Automatic measurements can help acquire statistical information about a jitter waveform. For example, an engineer might use this measurement to look at the performance of a phase-lock loop to determine if the stability period of a crystal is within specifications—or view the data valid window of a component's rise time, its duty cycle or pulse width.

Statistical Measurements

Digital oscilloscopes can also help evaluate measurements, like jitter or metastability, statistically. Some common statistical approaches to consider for debugging are:

- Mean Value is the average value (arithmetic mean) of a clock period. It is the reciprocal of the frequency.
- Standard Deviation is the average amount that a measurement varies from its mean value. It's useful for Gaussian processes, where the distribution is specified by the mean and standard deviation.
- Maximum, minimum and peak-peak values are observed during the measurement interval. Peak-peak value is the maximum value minus the minimum.
- Histograms plot the measurement values in the dataset against the frequency of occurrences in a measurement. It provides no order for events such as jitter, but does provide a good estimate of the probability of the event.

Summary

Digital oscilloscopes, like the DPO4000 and DPO7000 series, are debugging tools that are simplifying how engineers troubleshoot their embedded system designs. DPOs improve engineering design, verification and debug productivity. Features, like continuous waveform capture, provide insight into noise, glitches, crosstalk and other analog characteristics affecting logic states, rise time, setup and hold times deforming ideal digital pulses.

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